REMARKS/ARGUMENTS

Claims 2-9 and 12-20 are currently pending in the present patent application. Claims 8-9 and 12-20 have been amended, and claims 1, 10, and 11 were previously cancelled. In view of the remarks/arguments presented below, the Applicants' attorney requests that the Examiner withdraw all outstanding objections and rejections, and issue a notice of allowance. ***If after reviewing this response the Examiner does not allow all of the claims, then he/she is requested to phone the undersigned attorney to schedule an interview before issuing a subsequent action.***

Consideration of Reference Cited in an IDS

The Applicants' attorney thanks the Examiner for considering EP 0 295 751, which was cited in the IDS filed with the application on September 12, 2003.

But the Applicants' attorney notes that the Examiner has yet to indicate consideration of the European Search Report dated May 28, 2003, for European Patent Application No. EP 02 02 0689, filed in English in the same IDS on September 12, 2003. Therefore, the Applicants' attorney respectfully requests that the Examiner indicate consideration of this reference at the Examiner's earliest convenience by returning a copy of the IDS 1449 with the Examiner's initials next to all the references cited in this IDS.

Objections to the Specification, and Objections and 35 U.S.C. 112 1st Paragraph Rejection of the Claims, in the Office Action Mailed April 02, 2009

The Applicants' attorney thanks the Examiner for withdrawing these objections and rejection.

Examiner's Response to the Applicants' Attorney's Arguments in the Response Filed July 02, 2009

The Applicants' attorney effectively responds to the Examiner's arguments below in his responses to the Examiner's specific rejections of the claims. The Applicants' attorney, however, may provide no response where a claim amendment renders the Examiner's corresponding argument moot.

Rejection of Claims 8-9 and 12-14 Under 35 U.S.C. § 112 First Paragraph

The Applicants' attorney has amended claims 8 and 14, and these amendments overcome this rejection of claims 8-9 and 14.

But the Applicants' attorney disagrees that claims 12 and 13 fail to comply with the written description requirement.

Claim 12 recites a control circuit operable to cause an array of memory locations to operate as a random-access memory during all read operations, and as a first-in-first-out memory during all write operations.

For example, referring, *e.g.*, to FIGS. 3-4 and paragraphs [34] – [35] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable to cause an array of memory locations ELE to operate as a random-access memory per FIG. 4 by deasserting a control signal ST/RT (FIG. 2A), and to operate as a FIFO per FIG. 3 by asserting ST/RT. Consequently, it is at least inherent in the patent application that the control unit 105 may deassert ST/RT for each and every read operation such that the memory locations ELE "operate as a random-access memory during all read operations:" likewise, it is at least inherent in the patent application that the control unit 105 may assert ST/RT for each and every write operation such that the memory locations ELE operate "as a first-in-first-out memory during all write operations."

For at least these reasons, claims 12 and 13 meet the written description requirement.

Rejection of Claims 8-9 and 14 Under 35 U.S.C. § 112 Second Paragraph

The Applicants' attorney has amended claims 8 and 14, and these amendments overcome this rejection of claims 8-9 and 14.

Rejection of Claims 8-9 and 15-16 Under 35 U.S.C. § 102(e) as Being Anticipated By U.S. 6,578,109 to Stone

Claim 8

Claim 8 as amended recites a control circuit operable during a read operation to configure memory locations for random access only, and during a write operation to configure the memory locations for sequential access only.

For example, referring, *e.g.*, to FIGS. 3-4 and paragraphs [34] – [35] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable during a read operation to configure memory locations ELE for random access only (FIG. 4) by deasserting a control signal ST/RT (FIG. 2A), and is operable during a write operation to configure the memory locations ELE for sequential access only (FIG. 3) by asserting ST/RT.

In contrast, Stone does not disclose a control circuit operable during a read operation to configure memory locations for random access only, and during a write operation to configure the memory locations for sequential access only. Referring to FIG. 10 and col. 9, line 43 – col. 10, line 18, Stone's cache controller 516 configures the cache channels 520 for both random access and sequential access during read operations and during write operations in response to, e.g., a mode bit, from another circuit. Therefore, because Stone's cache controller 516 is "at the mercy" of the, *e.g.*, mode bit, the controller has not ability to configure memory locations for random access only or sequential access only.

Claim 9

This claim is patentable at least by virtue of its dependency from claim 8.

Claim 15

Claim 15 as amended recites during one of a read mode and a write mode of operation, configuring memory locations of a memory for random access only, and during the other of the read mode and the write mode of operation, configuring the memory locations for sequential access only.

For example, referring, *e.g.*, to FIGS. 3-4 and paragraphs [34] – [35] of the patent application, in an embodiment, during a read operation a control unit 105 (FIG. 1) configures memory locations ELE for random access only (FIG. 4) by deasserting a control signal ST/RT (FIG. 2A), and during a write operation the control unit 105 configures the memory locations ELE for sequential access only (FIG. 3) by asserting ST/RT.

In contrast, Stone does not disclose during one of a read mode and a write mode of operation, configuring memory locations of a memory for random access only, and during the other of the read mode and the write mode of operation, configuring the memory locations for sequential access only, for reasons similar to those recited above in support of the patentability of claim 8.

Claim 16

This claim is patentable at least by virtue of its dependency from claim 15.

Rejection of Claims 17-20 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Stone and U.S. 6,091,645 to Iadanza

As discussed above in support of the patentability of claim 15 in view of Stone, Stone does not disclose during one of a read mode and a write mode of operation, configuring memory locations of a memory for random access only, and during the other of the read mode and the write mode of operation, configuring the memory locations for sequential access only.

And it appears that Iadanza also does not disclose during one of a read mode and a write mode of operation, configuring memory locations of a memory for random access only, and during the other of the read mode and the write mode of operation, configuring the memory locations for sequential access only.

Consequently, because at least some of the limitations of claim 15 are omitted from both Stone and Iadanza, the combination of Stone and Iadanza does not support a prima facie case of obviousness against claims 17-20, which depend from claim 15.

Therefore, the combination of Stone and Iadanza does not render claims 17-20 obvious.

Rejection of Claims 8 and 14-16 Under 35 U.S.C. § 103(a) as Being Unpatentable Over U.S. 2002/0087817 to Tomaiuolo and U.S. 4,656,625 to Nojiri

Claim 8

Claim 8 as amended recites a control circuit operable during a read operation to configure memory locations for random access only, and during a write operation to configure the memory locations for sequential access only.

For example, referring, *e.g.*, to FIGS. 3-4 and paragraphs [34] – [35] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable during a read operation to configure memory locations ELE for random access only (FIG. 4) by deasserting a control signal ST/RT (FIG. 2A), and is operable during a write operation to configure the memory locations ELE for sequential access only (FIG. 3) by asserting ST/RT.

In contrast, the combination of Tomaiuolo and Nojiri does not render claim 8 obvious because neither Tomaiuolo nor Nojiri, alone or in combination, discloses or suggests a control circuit operable during a read operation to configure memory locations for random access only, and during a write operation to configure the memory locations for sequential access only.

Referring to paragraphs [0021]–[0022], it appears that Tomaiuolo discloses memory locations that are configured for both random access and sequential access

during read and write operations. Tomaiuolo's memory locations are accessed sequentially if a current address consecutive to a previous address is received, and are accessed randomly otherwise; that is, the type of access (sequential or random) depends on a received address. Consequently, Tomaiuolo actually teaches away from during a read operation, configuring memory locations for random access only, and during a write operation, configuring the memory locations for sequential access only, because such configuring of the memory locations would not allow the received address to dictate the type of memory access as taught by Tomaiuolo.

Similarly, referring to FIGS. 7 and 12(a) – 12(e) and col. 8, line 54 – col. 9, line 2, it appears that Nojiri also discloses memory locations (speech path memory (SPM) 24 of FIG. 7) that are configured for both random access and sequential access during read and write operations. For example, even during a write operation, the memory locations in Nojiri's SPM 24 may be randomly accessed by addressing (see the addresses in FIG. 12(c) that correspond to the data in FIG. 12(e) being written to the SPM 24). Consequently, Nojiri actually teaches away from during a read operation, configuring memory locations for random access only, and during a write operation, configuring the memory locations for sequential access only, because such configuring of the memory locations would not allow random write access of the SPM 24 as taught by Nojiri.

Consequently, because both Tomaiuolo and Nojiri fail to disclose or suggest at least one same limitation of claim 8, claim 8 is patentable over the combination of Tomaiuolo and Nojiri.

Claim 14

Claim 14 as amended recites a control circuit operable during a write operation to configure the memory locations for sequential access via a single one of the memory locations only.

For example, referring, *e.g.*, to FIG. 3 and paragraph [34] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable during a write operation to configure the memory locations ELE for sequential access via a single

one of the memory locations ELE [511] only (FIG. 3) by asserting a control signal ST/RT (FIG. 2A).

In contrast, neither Tomaiuolo nor Nojiri, alone or in combination, discloses or suggests a control circuit operable during a write operation to configure the memory locations for sequential access via a single one of the memory locations only.

Referring to paragraphs [0021]–[0022], it appears that Tomaiuolo discloses memory locations that, during a write operation, are configured for sequential access via multiple ones of the memory locations. During a write operation, Tomaiuolo's memory locations are accessed sequentially if a current address consecutive to a previous address is received. Therefore, because at least two addresses are required to initiate a sequential access, the memory locations are not configured for sequential access via a single memory location only. Consequently, Tomaiuolo actually teaches away from during a write operation, configuring memory locations for sequential access via a single one of the memory locations only, because such configuring of the memory locations would not allow Tomaiuolo's memory to operate as he describes.

Similarly, referring to FIGS. 7 and 12(a) – 12(e) and col. 8, line 54 – col. 9, line 2, it appears that Nojiri also discloses memory locations that, during a write operation, are configured for sequential access via multiple ones of the memory locations. During a write operation, the memory locations in Nojiri's SPM 24 are sequentially accessed by sequential addresses (see the addresses in FIG. 12(c) that correspond to the data in FIG. 12(e) being written to the SPM 24). Consequently, Nojiri actually teaches away from during a write operation, configuring the memory locations for sequential access via a single one of the memory locations only, because such configuring of the memory locations would not allow Nojiri's SPM 24 to operate as he describes.

Consequently, because both Tomaiuolo and Nojiri fail to disclose or suggest at least one same limitation of claim 14, claim 14 is patentable over the combination of Tomaiuolo and Nojiri.

Claim 15

Claim 15 as amended recites during one of a read mode and a write mode of operation, configuring memory locations of a memory for random access only, and during the other of the read mode and the write mode of operation, configuring the memory locations for sequential access only.

For example, referring, *e.g.*, to FIGS. 3-4 and paragraphs [34] – [35] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable during a read operation to configure memory locations ELE for random access only (FIG. 4) by deasserting a control signal ST/RT (FIG. 2A), and is operable during a write operation to configure the memory locations ELE for sequential access only (FIG. 3) by asserting ST/RT.

In contrast, neither Tomaiuolo nor Nojiri, alone or in combination, discloses or suggests during a read operation, configuring memory locations for random access only, and during a write operation, configuring the memory locations for sequential access only.

Referring to paragraphs [0021]–[0022], it appears that Tomaiuolo discloses configuring memory locations for both random access and sequential access during read and write operations. Tomaiuolo's memory locations are accessed sequentially if a current address consecutive to a previous address is received, and are accessed randomly otherwise; that is, the type of access (sequential or random) depends on a received address. Consequently, Tomaiuolo actually teaches away from during a read operation, configuring memory locations for random access only, and during a write operation, configuring the memory locations for sequential access only, because such configuring of the memory locations would not allow the received address to dictate the type of memory access as taught by Tomaiuolo.

Similarly, referring to FIGS. 7 and 12(a) – 12(e) and col. 8, line 54 – col. 9, line 2, it appears that Nojiri also discloses configuring memory locations (speech path memory (SPM) 24 of FIG. 7) for both random access and sequential access during read and write operations. For example, even during a write operation, the memory

locations in Nojiri's SPM 24 may be randomly accessed by addressing (see the addresses in FIG. 12(c) that correspond to the data in FIG. 12(e) being written to the SPM 24). Consequently, Nojiri actually teaches away from during a read operation, configuring memory locations for random access only, and during a write operation, configuring the memory locations for sequential access only, because such configuring of the memory locations would not allow random write access of the SPM 24 as taught by Nojiri.

Consequently, because both Tomaiuolo and Nojiri fail to disclose or suggest at least one same limitation of claim 15, claim 15 is patentable over the combination of Tomaiuolo and Nojiri.

Claim 16

This claim is patentable at least by virtue of its dependency from claim 15.

Rejection of Claims 2-7 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Iadanza, Applicant Admitted Prior Art (APA), and Stone

Claim 3

Claim 3 as previously pending recites an array configuration circuit for selectively placing at least one array of memory elements in one of two operating configurations, and a memory element access circuit, responsive to a memory address, for enabling access to a prescribed memory element in a selected sub-array of the memory elements after a prescribed number of shifts, depending on the memory address, of the data content of the memory elements in the selected sub-array.

For example, referring, *e.g.*, to FIG. 6 and paragraphs [40]-[53] of the patent application, in a embodiment, an array control circuit 205 (FIG. 2A, array configuration circuit) selectively places at least one array AR[1] (FIG. 5) of memory elements ELE[0:63] in a FIFO or in a random-access configuration (one of two operating configurations), and a comparator 603, logic gate 607, and mux 609 (together forming a memory element access circuit), responsive to a memory address RIN[4:6], for enabling access to the bottom memory element ELE[24] (a prescribed memory

element) in a selected sub-array ELE[24:31] after a prescribed number of shifts, depending on the memory address RIN[4:6], of the data content of the memory elements ELE[24:31] in the selected sub-array.

In contrast, the combination of Iadanza, the APA, and Stone does not render claim 3 unpatentable.

First, the Examiner is incorrect that Iadanza discloses a memory element access circuit, responsive to a memory address, for enabling access to a prescribed memory element in a selected sub-array of the memory elements after a prescribed number of shifts, depending on the memory address, of the data content of the memory elements in the selected sub-array. On p. 22 of the Office Action, the Examiner points to col. 22, lines 8-18, col. 33, lines 5-10, and col. 33, lines 20-24 of Iadanza as disclosing this limitation. But referring to FIGS. 1A, 1B, and 2B (the figures to which the pointed-to text refers), Iadanza shows only memory cells $48_{1,1}$ – $48_{1,n}$ configured as memory stacks. Although the data content of the memory elements forming such a stack may be shifted from one memory element to another within the stack, such shifting does not depend on a memory address. Indeed, a major purpose of a stack is to allow data storage without requiring a memory address for addressing a data-storage element.

Second, the Examiner is incorrect that the APA "discloses two operating configurations: a first operating configuration, in which the memory elements of the at least one array are coupled one to another to form a monodimensional sequentially accessible memory, and a second operating configuration, in which the memory elements in each sub-array are coupled to one another so as to form an independent monodimensional sequentially accessible memory block to provide a memory that can be accessed sequentially in a first-in, first-out manner and a memory that can be accessed randomly." In contrast, the APA states only that a memory may be either a FIFO ***or*** a RAM; there is nothing in the APA to indicate that a memory may be operated in either a FIFO or a RAM configuration.

Consequently, for at least the above reasons, the Examiner has failed to make out a prima facie case of obviousness for claim 3, and, therefore, must withdraw this rejection of claim 3.

Claims 2 and 4-7

As discussed above, claim 3 is patentable over the combination of Iadanza, APA, and Stone. Therefore, claims 2 and 4-7 are patentable at least by virtue of their dependencies from claim 3.

Rejection of Claims 12-13 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Tomaiuolo, Iadanza, and Stone

Claim 12

Claim 12 as amended recites a control circuit operable to cause an array of memory locations to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations, wherein the memory locations comprise rings of serially coupled memory locations, and wherein during the read mode of operation, the control circuit is operable to control each of the rings to shift the contents of each respective memory location in the ring to a respective next memory location in the ring.

For example, referring, *e.g.*, to FIGS. 3-4, and 6 and paragraphs [34] – [59] of the patent application, in an embodiment, a control unit 105 (FIG. 1) is operable to cause an array AR[1] (FIG. 5) of memory locations ELE[0:63] to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations, wherein the memory locations ELE comprise rings of serially coupled memory locations ELE[0:7], ELE[8:15], . . . , ELE[56:63], and wherein during the read mode of operation, the control unit 105 is operable to control each of the rings to shift the contents of each respective memory location ELE in the ring to a respective next memory location ELE in the ring.

In contrast, the combination of Tomaiuolo, Iadanza, and Stone does not render claim 12 obvious.

First, the Examiner is incorrect that Tomaiuolo discloses rings of serially coupled memory locations. Referring to FIG. 2, Tomoaiuolo discloses only interlaced memory banks EVEN and ODD, but does not disclose memory locations arranged in rings.

Second, Iadanza does not disclose shifting the contents of each respective memory location in a ring to a respective next memory location in the ring while the memory locations are operating as a random-access memory. Referring to col. 10, lines 10-29, Iadanza at best appears to disclose shifting contents of a memory location in a ring to a next memory location in the ring while the memory locations are operating as a FIFO or a LIFO; FIFOs and LIFOs are not random-access memories.

Third, the Examiner is incorrect that Stone discloses a control circuit operable to cause an array of memory locations to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations. Referring to col. 9, line 40 – col. 10, line 7, Stone's cache controller 516 performs either a FIFO or random-access read operation depending on, *e.g.*, a mode bit, included in the read request; similarly, Stone's cache controller 516 performs either a FIFO or random-access write operation depending on, *e.g.*, a mode bit, included in the write request. Therefore, Stone's cache controller 516 is not operable to cause an array of memory locations to operate as a random-access memory during all read operations and a first-in-first-out memory during all write operations because the cache controller 516 is at the mercy of, *e.g.*, a mode bit, provided by another circuit.

Consequently, for at least the above reasons, the Examiner has failed to make out a prima facie case of obviousness for claim 12, and, therefore, must withdraw this rejection of claim 12.

Claim 13

As discussed above, claim 12 is patentable over the combination of Tomaiuolo, Iadanza, and Stone. Therefore, claim 13 is patentable at least by virtue of its dependency from claim 13.

CONCLUSION

The absence of additional patentability arguments should not be construed as either a disclaimer of such arguments or that such arguments are not believed to be meritorious. The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicants respectfully request the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.**

If the need for any fee in addition to any fee paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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